SECTION 8

TERMINOLOGIE

TERMINOLOGIE

A

ASCII

Sigle de USA Standard Code for Information Interchange.

ASYNCHRONE

Commande d'un dispositif de commutation par un signal relaxé qui déclenche les instructions successives, l'exécution d'une instruction déclenchant la suivante. La durée de chaque cycle n'est pas déterminée.

ADRESS LINE / BUS D'ADRESSES

La combinaison logique de Ø et de 1 sur ces lignes détermine à quel dispositif I/O où à quelle position de mémoire on s'adresse.

B

BCD (Binary Coded Decimal)

Chaque chiffre décimal est codé binairement dans des mots de 4 bits.La valeur binaire de ce mot correspond à la valeur du chiffre décimal. En code BCD, le nombre 11 serait 0001 0001. Connu également sous l'appellation de code 8421.

BIDIRECTIONNEL

Terme désignant un "port" ou un bus pouvant transmettre des données dans les deux directions.

BIT

Une ligne simple représentée par deux états logiques, soit un 1 ou un 0.

BINAIRE

Système de nombres utilisant 2 comme base par opposition au système décimal qui a pour base 10. Le système binaire ne requiert que 2 symboles, Ø et 1. En système binaire, deux est représenté par le nombre 10 (se lit un, zéro). Chaque chiffre après le premier 1 est multiplié par la base 2. La tabelle ci-après indique les dix premiers nombres dans les deux systèmes décimal et binaire :

Décimal	Binaire
0	0
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001

BUFFER / TAMPON

Circuit intercalé entre d'autres éléments de circuit pour éviter des interactions, pour adapter des impédances en vue de fournir des possibilités de commande supplémentaires ou pour différer la circulation des informations. Les tampons peuvent être inversés ou non inversés.

BUS DRIVER / AMPLIFICATEUR DE BUS

Circuit intégré branché sur le système du bus de données pour assurer une commande correcte des mémoires par le CPU lorsque plusieurs mémoires dépendent du même bus. Celles-ci sont nécessaires, étant donné la charge capacitive qui ralentit le débit des données et entrave le déroulement séquentiel des opérations du microprocesseur.

BUS SYSTEME / SYSTEME DE BUS

Il s'agit d'un réseau de pistes à l'intérieur du microprocesseur qui facilite la circulation des données. Les bus les plus importants d'un microprocesseur s'appellent Data Bus, Adress Bus et Control Bus.

BYTE / OCTET

Indique un nombre prédéterminé de bits consécutifs traités en tant qu'entité. Par exemple, bytes de 4 bits ou de 8 bits. "MOT" et "BYTE" sont utilisés indifféremment l'un pour l'autre.

C

CLOCK / HORLOGE

Générateur d'impulsions commandant la synchronisation des circuits de commutation dans un microprocesseur. La fréquence des impulsions d'horloge ne constitue pas le seul critère de la vitesse de traitement des données. Une bonne architecture du matériel et une habile programmation sont plus importantes. La plupart des microprocesseurs doivent disposer d'une horloge et les horloges multiphasées sont propres aux processeurs MOS.

CPU/Central Processing Unit / Microprocesseur Central)

Centre principal de calcul et coeur de tout ordinateur. La construction fondamentale du CPU comporte des éléments mémoires, appelés registres, des circuits de calcul dans le dispositif ALU (unité arithmétique et logique), le bloc de commande et I/O. Dès que la technologie LSI (Large Scale Integration) a permis de bâtir un CPU sur un seul IC chip, ce fut l'avènement du microprocesseur. Les microprocesseurs à un chip ne disposant que d'une mémoire limitée, des modules sont ajoutés pour compléter la capacité de mémorisation. La plupart des microprocesseurs courants se composent d'une série de circuits intégrés, l'un ou deux de ceux-ci formant le CPU.

E

D

DATA BUS / BUS DE DONNEES

Pour la communication à l'intérieur et vers l'extérieur, le microprocesseur utilise un bus de données. Celui-ci est bidirectionnel et peut transmettre des données depuis et vers le CPU, la mémoire et les dispositifs périphériques.

E

EXECUTION TIME / DUREE D'EXECUTION

Exprimée généralement en cycles d'horloge qui sont nécessaires pour exécuter une instruction. Comme la fréquence des impulsions d'horloge est connue, le temps d'exécution peut être calculé. Les fréquences d'impulsions peuvent être modifiées.

F

FIRMWARE

Les instructions du logiciel qui sont définitivement programmées dans une ROM sont souvent appelées Firmware.

H

HANDSHAKING

Expression familière désignant la méthode utilisée par un modem pour établir le contact avec un autre modem à l'autre bout de la ligne téléphonique. Ce terme est souvent utilisé dans le sens de tampon et interface, la seule différence étant que "handshaking" se réfère à une connection en paquet, quel que soit le circuit utilisé.

HARDWARE

Les composants individuels d'un circuit, passifs et actifs, furent longtemps désignés dans le jargon anglais des ingénieurs par le terme de hardware.
De nos jours toutes les pièces constituant les équipements de traitement de données sont englobées sous cette appellation générale.

HEXADECIMAL

Nombres entiers en notation à plusieurs chiffres, utilisant la base 16. (c.c. octal). Comme on a 16 chiffres hexadécimaux (0 à 15) et qu'il n'y a que 10 chiffres numériques (0 à 9), six chiffres supplémentaires représentant 10 à 15 doivent être introduits. A cet effet, on a eu recours aux six premières lettres de l'alphabet et les chiffres hexadécimaux se lisent donc comme suit : 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F. Le nombre décimal 16 devient 10 en hexadécimal. Le nombre décimal 26 devient 1A en hexadécimal.

HIGH ORDER (MSB = Most Significant Bit)

Indique un bit ou un groupe de bits de poids "FORT".

I

INTERFACE

Désigne une limite commune entre deux composants circuits ou systèmes voisins, conçue de telle façon à permettre l'échange d'informations entre les deux composants. Il faut malheureusement regretter que le terme "interface" soit confondu dans le langage courant avec buffer, handshake et adapter.

INSTRUCTION SET / LISTE DES INSTRUCTIONS

Constitue la liste complète des instructions pouvant être effectuées par un microprocesseur.

INTERRUPT / INTERRUPTION

Une interruption entraîne l'arrêt de la routine normale d'un microprocesseur pour pouvoir donner suite à un ordre de travail soudain. L'importance de la capacité d'interruption dépend du champ d'application pour lequel il a été prévu. Lorsqu'un certain nombre d'unités périphériques se trouvent à la limite du microprocesseur, il arrivera fréquemment que plusieurs interruptions simultanées se produisent. Pour permettre une interruption multiple, le processeur doit être en mesure d'accomplir les tâches suivantes : retarder ou empêcher d'autres interruptions ; interférer dans une interruption pour y introduire une interruption encore plus urgente; établir une méthode de priorité des interruptions; et, à la fin du travail d'interruption, rétablir la routine interrompue à son point d'arrêt.

I/O (Input/Output = Entrée/Sortie)

Contacts du circuit intégré reliés directement au système de bus interne, pour permettre au microprocesseur de communiquer avec le monde extérieur.

L

LOGIC / LOGIQUE

Procédé de traitement mathématique de logique formelle utilisant un système de symboles pour représenter les quantités et les rapports. Les symboles, ou fonctions logiques, sont ET, OU, NON, etc. Pour ne mentionner que quelques exemples (souvent en anglais AND, OR, NOT, etc.) Chaque fonction peut être traduite dans un circuit de commutation communément appelé "porte".Comme un commutateur (ou porte) n'a que deux états - ouvert ou fermé - il est possible d'avoir recours à des nombres binaires pour la solution des problèmes. Les fonctions logiques fondamentales obtenues par les circuits portes constituent la base de tout ordinateur élaboré.

E

L

LOW ORDER (LSB = LEAST SIGNIFICANT BIT)

Indique un bit ou un groupe de bits de poids "FAIBLE".

M

MEMORY / MEMOIRE

Partie d'un système de computer dans lequel des informations peuvent être entreposées pour un usage futur. Stockage et mémoire (en anglais "storage" and memory") sont des termes interchangeables. Les mémoires n'acceptent et ne gardent que les nombres binaires. Il existe des mémoires à tores (core memory), à disque (disk memory), à tambour (drum memory) et à semi-conducteur (semiconductor memory).

MOS (Metal Oxide Semiconductor)

La structure d'un transistor MOS à effet de champ (Field Effect Transistor = FET) est du métal sur de l'oxyde de silicium sur du silicium. L'électrode de métal est la porte; l'oxyde de silicium est l'isolateur et les régions porteuses dans le substrat de silicium deviennent drain et source. Il en résulte une sorte de sandwich semblable à un condensateur, ce qui explique pourquoi le MOS est plus lent que le bipolaire, puisque le condensateur sandwich doit déjà se charger avant de laisser passe le courant. Les trois grands avantages du MOS sont la simplicité de sa production par suite des phases réduites de la fabrication, le faible encombrement du chip qui offre une grande densité fonctionnelle et l'interconnexion très aisée sur le chip. Ces particularités ont permis au MOS de vaincre la barrière de la LSI, à laquelle la technique bipolaire commence seulement à s'attaquer. La calculatarice de poche et le microprocesseur représentent des triomphes de la technique MOS-LSI.

MICROPROCESSEUR

Le microprocesseur est une unité de traitement fabriquée sur un ou deux chips. Quoique cela ne soit pas visible de l'extérieur, ils renferment tous des secteurs bien définis : unité arithmétique et logique (ALU), bloc de commande et bloc registre. Lorsque ces unités sont combinées avec un système de mémoire, il est d'usage de nos jours d'appeler un tel ensemble un microprocesseur.
Il faut ajouter que chaque microprocesseur est livré avec une liste d'instructions qui, pour l'usager, est certainement aussi utile que le hardware.

MULTIPLEXAGE

Le multiplexage est un procédé permettant de transmettre simultanément plus d'un signal sur une même connexion. Des deux méthodes en usage, l'une partage la largeur de la bande du canal au niveau de la fréquence, tout comme des coureurs de haies courent et sautent dans les bandes qui leur sont assignées, permettant ainsi à plusieurs concurrents d'être présents sur une mêm piste.
La seconde méthode consiste à partager le canal dans le temps par rapport aux différents signaux, à l'image des sauteurs à la perche qui sautent l'un après l'autre par-dessus la même barre. On pourrait désigner les deux méthodes comme

E

traitement en parallèle ou en série. Le multiplexage dans le temps pourrait paraître non "simultané", mais il faut se souvenir que la vitesse du signal est si rapide qu'il est possible de multiplexer quatre nombres différents par un décodeur-ampli et de les voir s'afficher sur quatre écrans différents sans que l'oeil soit incommodé par le moindre scintillement.

P

PARALLEL OPERATION / TRAITEMENT PARALLELE

Traitement simultané de tous les chiffres d'un mot ou byte par transmission de chaque chiffre sur un canal ou une ligne de bus séparé.

PORT

Terminaux des dispositifs qui assurent l'accès électrique à un système ou à un circuit. Point auquel I/O entre en contact avec l'extérieur.

PROGRAMME

Procédure servant à résoudre un problème, souvent appelée Software.

R

RAM (Random Access Memory)

Mémoire à accès sélectif, en ce sens que l'accès, à n'importe quelle position de la mémoire, est immédiatement possible, grâce à des coordonnées verticales et horizontales. L'information peut être "lue" ou "écrite" tout aussi rapidement.

READ / LIRE

Partie du cycle d'instruction, lorsque le microprocesseur lit des informations d'une mémoire déterminée ou d'un dispositif I/O.

REGISTRE

Un registre est une mémoire de plus petite envergure. Les mots qui y sont stockés peuvent servir à des opérations arithmétiques, logiques ou de transfert. La mémorisation dans des registres peut être temporaire et leur grand intérêt réside dans l'accessibilité qu'elles offrent au CPU. La quantité de registres d'un microprocesseur est considéré comme l'un des atouts essentiels de son architecture.

ROM (Read Only Memory) /MEMOIRE MORTE UTILISEE EN LECTURE

A l'état brut, une ROM est constituée par une mosaïque de cellules indifférenciées. Un type de ROM est programmée par application d'un masque au dernier stade de la fabrication. Un autre type de mémoires, plus connues sous l'appellation de PROM, peuvent être programmées par l'utilisateur à l'aide d'un équipement adéquat. Les programmes mémorisés dans des PROM sont souvent

E

qualifiés de Firmware, car ils ne peuvent plus être modifiés. Toutefois, il existe maintenant sur le marché des mémoires programmables effaçables par irradiation d'ultraviolets et reprogrammables électriquement (EPROM).

SOFTWARE

Ce que la partition est au piano, la Software l'est au computer. Considéré du point de vue pratique, on peut dire que la Software est le manuel d'instructions de l'ordinateur. Ce nom a évidemment été choisi pour contraster avec le célèbre Hardware que connurent les premiers programmeurs. Le Software est le langage utilisé par le programmeur pour communiquer avec l'ordinateur. Comme le seul langage compris par l'ordinateur est mathématique, le programmeur doit transformer ses instructions verbales en nombres. En ce qui concerne les microprocesseurs, qui diffèrent selon les producteurs, des bibliothèques de Software sont élaborées par le fabricant pour répondre aux besoins des usagers.

STORAGE

Le terme de "storage" est interchangeable avec celui de "memory". En fait, ce vocable est utilisé de préférence par les personnes qui veulent éviter de voir une analogie entre une fonction de l'ordinateur et le cerveau humain.

W

WRITE / ECRIRE

Partie du cycle d'instruction durant laquelle le microprocesseur écrit dans une position de mémoire ou un dispositif I/O.

WORD / MOT

Groupe de caractères traité en tant qu'ensemble, se trouvant dans une position de mémoire déterminée.
En somme, un byte est un groupe de bits par rapport à un mot qui est un groupe de caractères et de symboles numériques et/ou alphabétiques, mais les deux termes sont en fait couramment utilisés l'un pour l'autre.

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E

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LOC  OBJ    LINE          SOURCE STATEMENT

4000        = 144 OUTS1   EQU  4000H          ;TRANSFERT A SLAVE 1
4003        = 145 INS1    EQU  OUTS1+3        ;INPUT PORT 1, SLAVE 1 ET 2
4006        = 146 OUTS2   EQU  INS1+3         ;TRANSFERT A SLAVE 2
4009        = 147 INS2    EQU  OUTS2+3        ;TRANSFERT DE SLAVE 2
400C        = 148 KBCOD1  EQU  INS2+3         ;CODE CLAVIER
400D        = 149 KBCOD2  EQU  KBCOD1+1       ;CODE CARACTERE
400E        = 150 KBCNT   EQU  KBCOD2+1       ;COMPTEUR SHIFT CODE CLAVIER
400F        = 151 KBSHT   EQU  KBCNT+1        ;SHIFT CODE CLAVIER
4010        = 152 KBDEA   EQU  KBSHT+1        ;CODE TOUCHE MORTE
4011        = 153 KBFCT   EQU  KBDEA+1        ;CODE FONCTION CLAVIER
4012        = 154 CAPIT   EQU  KBFCT+1        ;PAS EN ECRITURE COMPOSEE
4013        = 155 DAVER   EQU  CAPIT+1        ;SELECTEUR VARIANTE DAISY
4014        = 156 HAINT   EQU  DAVER+1        ;SELECTEUR FORCE DE FRAPPE
4015        = 157 SELF    EQU  HAINT+1        ;SELECTEUR LINE FEED
4016        = 158 MODE    EQU  SELF+1         ;SELECTEUR MODE JUSTIFICATION
4017        = 159 PITCH   EQU  MODE+1         ;SELECTEUR DE PAS
4018        = 160 SHEM    EQU  PITCH+1        ;SELECTION MODE MEMOIRE
4019        = 161 ADMEM   EQU  SHEM+1         ;SELECTION ADRESSE MEMOIRE
401A        = 162 HTPOIN  EQU  ADMEM+1        ;POINTEUR DE HTAB
401C        = 163 ECHT    EQU  HTPOIN+2       ;ECHAPPEMENT
401D        = 164 FFRP    EQU  ECHT+1         ;FORCE DE FRAPPE
            = 165 ;
            = 166 ;
401E        = 167 ADFL1   EQU  FFRP+1         ;FLAGS
            = 168 ;
0001        = 169 FREP    EQU  00000001B      ;FLAG REPETITION
0002        = 170 FVFCT   EQU  00000010B      ;FLAG VERROUILLAGE FONCTIONS
0004        = 171 FVM     EQU  00000100B      ;FLAG MARGE VARIABLE
0008        = 172 FWS     EQU  00001000B      ;FLAG NON ENREG. MEM. LIGNE
0010        = 173 FBOLD   EQU  00010000B      ;FLAG BOLD
0020        = 174 FUNDS   EQU  00100000B      ;FLAG SOULIGNEMENT
0040        = 175 FBOLDA  EQU  01000000B      ;FLAG BOLD AUX.
0080        = 176 FUNDA   EQU  10000000B      ;FLAG SOULIGNEMENT AUX.
            = 177 ;
            = 178 ;
401F        = 179 ADFL2   EQU  ADFL1+1        ;FLAGS
            = 180 ;
0001        = 181 FDEAK   EQU  00000001B      ;FLAG TOUCHE MORTE
0002        = 182 FVISU   EQU  00000010B      ;FLAG VISUALISATION
0004        = 183 FWFMT   EQU  00000100B      ;FLAG ENREGISTREMENT FORMAT X-Y
0008        = 184 FWTEX   EQU  00001000B      ;FLAG ENREGISTREMENT TEXTE
0010        = 185 FRFMT   EQU  00010000B      ;FLAG IMPRESSION FORMAT X-Y
0020        = 186 FRTEX   EQU  00100000B      ;FLAG IMPRESSION TEXTE
0040        = 187 FRETA   EQU  01000000B      ;FLAG RETOUR AUTOMATIQUE
0080        = 188 FZMARD  EQU  10000000B      ;FLAG ZONE MARGE DROITE
            = 189 ;
            = 190 ;
4020        = 191 ADFL3   EQU  ADFL2+1        ;FLAGS
            = 192 ;
0001        = 193 FCENT   EQU  00000001B      ;FLAG DE CENTRAGE
0002        = 194 FCENTR  EQU  00000010B      ;FLAG CENTRAGE SUR MARGE DROITE
0004        = 195 FDETA   EQU  00000100B      ;FLAG TABULATION DECIMALE
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LOC  OBJ   LINE          SOURCE STATEMENT

0008       = 196 FDISP   EQU  00001000B      ;FLAG DISPLAY ON
0010       = 197 FPADEC  EQU  00010000B      ;FLAG PARAGRAPHE DECALE
0020       = 198 FBELL1  EQU  00100000B      ;FLAG ALARME ACCOUSTIQUE
0040       = 199 FBELL2  EQU  01000000B      ;FLAG SIGNAL ACCOUSTIQUE
0080       = 200 FSPR    EQU  10000000B      ;FLAG SUPPRESSION PRINT CARACTERE
           = 201 ;
4021       = 202 ADFL4   EQU  ADFL3+1        ;FLAGS
           = 203 ;
0001       = 204 FDISAV  EQU  00000001B      ;FLAG DEVALIDATION TRANSFERT AV.
0002       = 205 FREPA   EQU  00000010B      ;FLAG REMISE EN PAGE
0004       = 206 FSTOP   EQU  00000100B      ;FLAG ETAT STOP IMPRESSION
0008       = 207 FDISBK  EQU  00001000B      ;FLAG SAUVETAGE ETAT DISPLAY
0010       = 208 FBLDAR  EQU  00010000B      ;FLAG GRAS AUX. ARRIERE
0020       = 209 FUNDAR  EQU  00100000B      ;FLAG SOULIGNEMENT AUX. ARRIERE
0040       = 210 FBLDAV  EQU  01000000B      ;FLAG GRAS AUX. AVANT
0080       = 211 FUNDAV  EQU  10000000B      ;FLAG SOULIGNEMENT AUX. AVANT
           = 212 ;
4022       = 213 CDESEL  EQU  ADFL4+1        ;CODE COMMANDE SELECT. SOULIGN.
4023       = 214 CAPOS   EQU  CDESEL+1       ;POSITION CAVALIER
4025       = 215 SAUSP   EQU  CAPOS+2        ;SAUVETAGE DE SP
4027       = 216 ADML    EQU  SAUSP+2        ;ADRESSE TEMP.MEM.LIGNE
4029       = 217 PMEM    EQU  ADML+2         ;POINTEUR DEBUT MEMOIRE X
402B       = 218 PMED    EQU  PMEM+2         ;POINTEUR DEBUT PARTIE VIDE
402D       = 219 PMEF    EQU  PMED+2         ;POINTEUR FIN PARTIE VIDE
402F       = 220 PLECF   EQU  PMEF+2         ;POINTEUR LECTURE MEMOIRE FORMAT
4031       = 221 PMEMF   EQU  PLECF+2        ;POINTEUR DEBUT MEMOIRE FORMAT
4033       = 222 PENDF   EQU  PMEMF+2        ;POINTEUR FIN MEMOIRE FORMAT
4035       = 223 POSCHA  EQU  PENDF+2        ;POSITION DESTINATION CHARIOT
4038       = 224 PENDX   EQU  POSCHA+3       ;POINTEUR FIN MEMOIRE X
403A       = 225 PENDT   EQU  PENDX+2        ;POINTEUR FIN MEMOIRE TEXTE
403C       = 226 MEMNB   EQU  PENDT+2        ;NO. ZONE MEMOIRE
403D       = 227 MSPACE  EQU  MEMNB+1        ;CAPACITE RESTANTE MEMOIRE TEXTE
403F       = 228 PCENTL  EQU  MSPACE+2       ;POINTEUR CENTRAGE GAUCHE M.L.
4041       = 229 PCENTR  EQU  PCENTL+2       ;POINTEUR CENTRAGE DROITE M.L.
4043       = 230 PPCENT  EQU  PCENTR+2       ;POINTEUR POS.CENTRAGE
4045       = 231 PRPOS   EQU  PPCENT+2       ;POSITION CHARIOT
4047       = 232 PPLNM   EQU  PRPOS+2        ;POS.CARACTERE POINTE PAR PLINM
4049       = 233 PPRINT  EQU  PPLNM+2        ;POINTEUR POS.A IMPRIMER
404B       = 234 PSTART  EQU  PPRINT+2       ;REFERENCE DISPLAY DANS MEM. LIGNE
404D       = 235 PLINM   EQU  PSTART+2       ;POINTEUR MEMOIRE LIGNE
404F       = 236 TLINM   EQU  PLINM+2        ;POINTEUR MEMOIRE LIGNE TEMP.
4051       = 237 BLINM   EQU  TLINM+2        ;POINTEUR MEMOIRE LIGNE TEMP.
4053       = 238 TEMP1   EQU  BLINM+2        ;POINTEUR MEMOIRE LIGNE TEMP.
4055       = 239 TEMP2   EQU  TEMP1+2        ;POINTEUR MEMOIRE LIGNE TEMP.
4057       = 240 PDEPL   EQU  TEMP2+2        ;POINT. DERNIER EL. PRINT. LIGNE
4059       = 241 PWIND   EQU  PDEPL+2        ;DEBUT FENETRE DISPLAY
405B       = 242 PIMT    EQU  PWIND+2        ;POINTEUR SORTIE MEMOIRE LIGNE
405D       = 243 RIDIM   EQU  PIMT+2         ;RECADRAGE DISPLAY
405E       = 244 SON     EQU  RIDIM+1        ;MARQUE SONNETTE
405F       = 245 CURS    EQU  SON+1          ;CURSEUR DISPLAY
4060       = 246 DIRAM   EQU  CURS+1         ;BASE DE MEMOIRE DISPLAY
408A       = 247 RSON    EQU  DIRAM+42       ;ENREGISTREMENT SON
408B       = 248 RCURS   EQU  RSON+1         ;ENREG. CURS
408C       = 249 DIRAC   EQU  RCURS+1        ;MEM. DISPLAY AUX.
40B6       = 250 SPACE1  EQU  DIRAC+42       ;CAP. RESTANTE MEM. CENTAINES
40B7       = 251 SPACE2  EQU  SPACE1+1       ;IDEM, DIZAINES
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40B8      = 252 SPACE3  EQU  SPACE2+1        ;IDEM, UNITES
40B9      = 253 AMARG   EQU  SPACE3+1        ;ADR. MARGE GAUCHE (TEMP.)
40BB      = 254 LINEM   EQU  AMARG+2         ;MEMOIRE LIGNE
4275      = 255 ENDLM   EQU  LINEM+442       ;FIN MEMOIRE LIGNE
42DC      = 256 STACKO  EQU  ENDLM+2+101     ;STACK
42DD      = 257 PFAIL   EQU  STACKO+1        ;TEST STANDBY
42DF      = 258 PAPOS   EQU  PFAIL+2         ;POSITION PAPIER
42E0      = 259 INDMA   EQU  PAPOS+1         ;MARGEUR INDENT
42E2      = 260 LEFMA   EQU  INDMA+2         ;MARGEUR GAUCHE
42E4      = 261 HTAB    EQU  LEFMA+2         ;CAVALIERS DE TABULATION HORIZONTALE
4320      = 262 RIGHM   EQU  HTAB+60         ;MARGEUR DROITE
4322      = 263 VTAB    EQU  RIGHM+2         ;CAVALIER DE TABULATION VERTICALE
4323      = 264 TOPWS   EQU  VTAB+1          ;MEMOIRE UTILISATEUR
4FFF      = 265 EOM     EQU  4FFFH           ;FIN MEMOIRE UTILISATEUR
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DONNEES TECHNIQUES

E

intel

8085

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

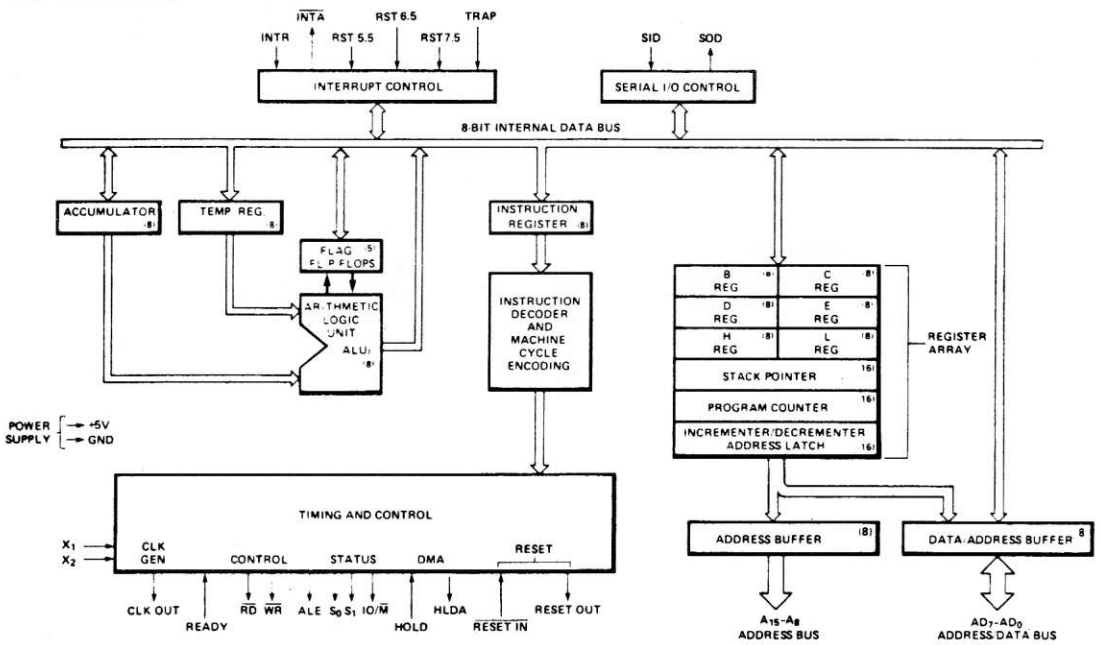
- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle**
- **On-Chip Clock Generator (with External Crystal or RC Network)**
- **On-Chip System Controller**
- **Four Vectored Interrupts (One is non-Maskable)**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64K Bytes of Memory**

The Intel® 8085 is a new generation, complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085 (CPU), 8156 (RAM) and 8355/8755 (ROM/PROM).

The 8085 incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080, thereby offering a high level of system integration.

The 8085 uses a multiplexed Data Bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8355 8755 memory products allows a direct interface with 8085.

8085 CPU FUNCTIONAL BLOCK DIAGRAM



8085 FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

A_8-A_{15} (Output 3-State)

Address Bus: The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes.

AD_{0-7} (Input/Output 3-state)

Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles.

3-stated during Hold and Halt modes.

ALE (Output 3-state)

Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. 3-stated during Hold and Halt modes.

S0, S1 (Output)

Data Bus Status. Encoded status of the bus cycle:

S_1	S_0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S_1 can be used as an advanced R/$\overline{W}$ status.

$\overline{RD}$ (Output 3-state)

READ; indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. Tri-stated during Hold and Halt.

$\overline{WR}$ (Output 3-state)

WRITE, indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. Tri-stated during Hold and Halt modes.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input)

HOLD; indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, and ALE lines are tri-stated.

HLDA (Output)

HOLD ACKNOWLEDGE; indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low.

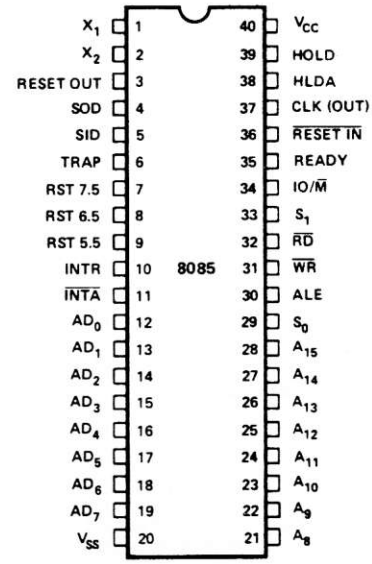


Figure 1. 8085 PINOUT DIAGRAM

INTR (Input)

INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{INTA}$ (Output)

INTERRUPT ACKNOWLEDGE; is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.

RST 5.5
RST 6.5
RST 7.5] (Inputs)

RESTART INTERRUPTS; These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 → Highest Priority
RST 6.5
RST 5.5 → Lowest Priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

TRAP (Input)

Trap interrupt is a nonmaskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

$\overline{\text{RESET IN}}$ (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X_1, X_2 (Input)

Crystal or R/C network connections to set the internal clock generator. X1 can also be an external clock input instead of a crystal.

CLK (Output)

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU.

IO/$\overline{\text{M}}$ (Output)

IO/$\overline{\text{M}}$ indicates whether the Read-Write is to memory or I/O. Tri-stated during Hold and Halt modes.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

V_{CC}

+5 volt supply.

V_{SS}

Ground Reference.

FUNCTIONAL DESCRIPTION

The 8085 is a complete 8 bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz thus improving on the present 8080's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU, a RAM-IO, and a ROM or PROM/IO chip.

The 8085 uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower 8-bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The 8085 provides $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{Memory}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. Hold, Ready, and all Interrupts are synchronized. The 8085 also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the 8085 has three maskable, restart interrupts and one nonmaskable trap interrupt.

8085 vs. 8080

The 8085 includes the following features on-chip in addition to all of the 8080 functions.

a. Internal clock generator
b. Clock output
c. Fully synchronized Ready
d. Schmitt action on $\overline{\text{RESET IN}}$
e. RESET OUT pin
f. $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{M}}$ Bus Control Signals
g. Encoded Status information
h. Multiplexed Address and Data
i. Direct Restarts and nonmaskable Interrupt
j. Serial Input/Output lines

The internal clock generator requires an external crystal or R-C network. It will oscillate at twice the basic CPU operating frequency. A 50% duty cycle, two phase, nonoverlapping clock is generated from this oscillator internally and one phase of the clock ($\phi 2$) is available as an external clock. The 8085 directly provides the external RDY synchronization previously provided by the 8224. The $\overline{\text{RESET IN}}$ input is provided with a Schmitt action input so that power-on reset only requires a resistor and capacitor. RESET OUT is provided for System RESET.

The 8085 provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ signals for Bus control. An $\overline{\text{INTA}}$ which was previously provided by the 8228 in 8080 system is also included in 8085.

STATUS INFORMATION

Status information is directly available from the 8085. *ALE serves as a status strobe.* The status is partially encoded and provides the user with advanced timing of the type of bus transfer being done. IO $\overline{\text{M}}$ cycle status signal is provided directly also. Decoded S_0, S_1 carries the following status information:

	S_1	S_0
HALT	0	0
WRITE	0	1
READ	1	0
FETCH	1	1

S1 can be interpreted as R/$\overline{\text{W}}$ in all bus transfers.

In the 8085 the 8 LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees extra pins for expanded interrupt capability.

INTERRUPT AND SERIAL I/O

The 8085 has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080 INT. Each of three RESTART inputs, 5.5, 6.5, 7.5, has a programmable mask. TRAP is also a RESTART interrupt **except it is non-maskable.**

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

Name	RESTART Address (Hex)
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip flop which generates the internal interrupt request. The RST 7.5 request flip flop remains set until the request is serviced. Then it is reset automatically. This flip flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085. The RST 7.5 internal flip flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP - highest priority, RST 7.5, RST 6.5, RST 5.5, INTR - lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and

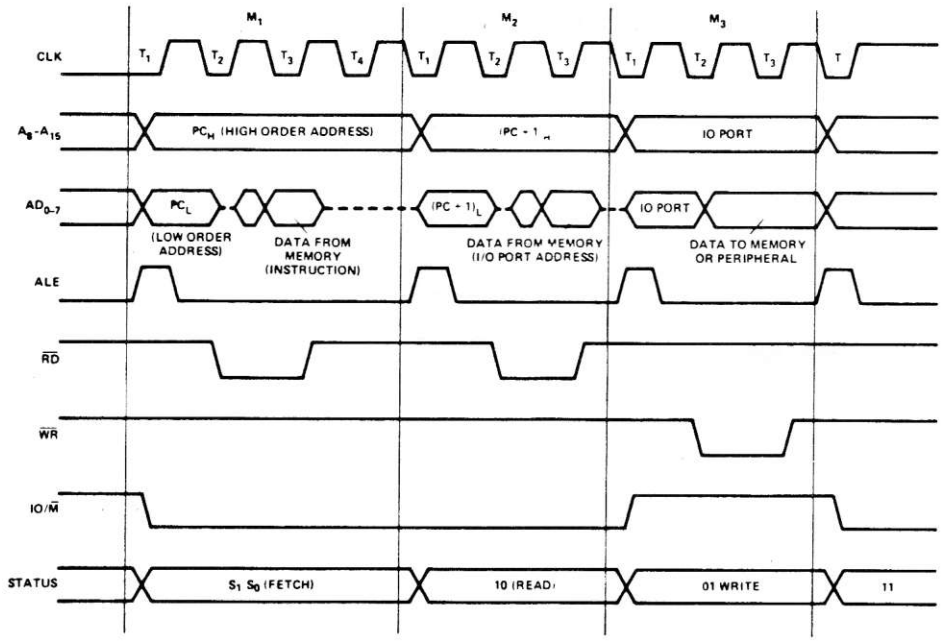
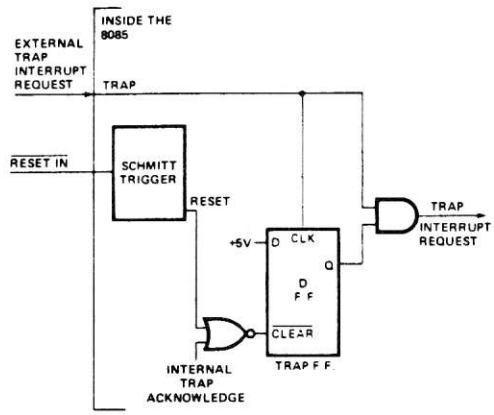


FIGURE 2. 8085 BASIC SYSTEM TIMING.

remain high to be acknowledged, but will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches.

The following diagram illustrates the TRAP interrupt request circuitry within the 8085.



Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

Since a TRAP interrupt can occur and disable the other interrupts whether they were previously enabled or not, it is not possible to restore the previous interrupt enable status following a TRAP.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

BASIC SYSTEM TIMING

The 8085 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OUT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085 can be used with slow memory. Hold causes the CPU to relinguish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

8085 family includes memory components, which are directly compatible to the 8085 CPU. For example, a system consisting of the three chips, 8085, 8156, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 3.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 4 shows the system configuration of Memory Mapped I/O using 8085.

The 8085 CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 5.

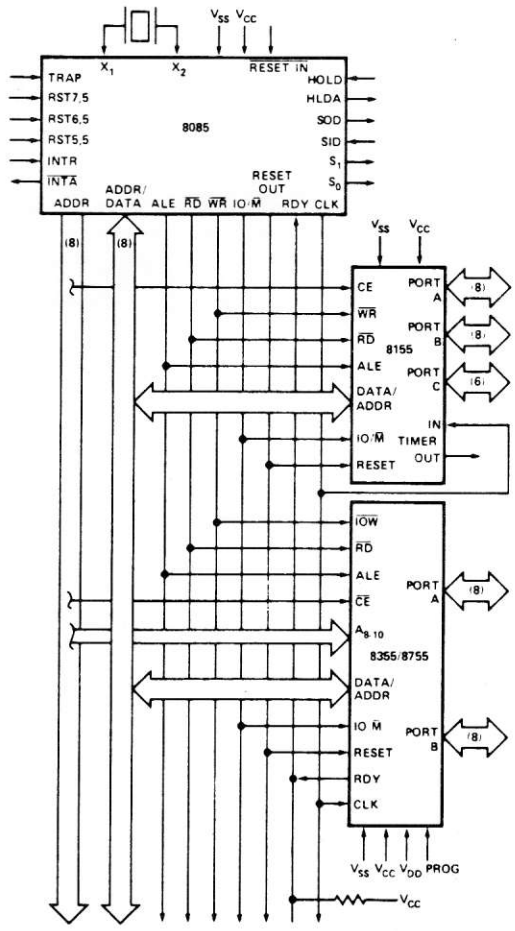


FIGURE 3. 8085 MINIMUM SYSTEM (STANDARD I/O TECHNIQUE)

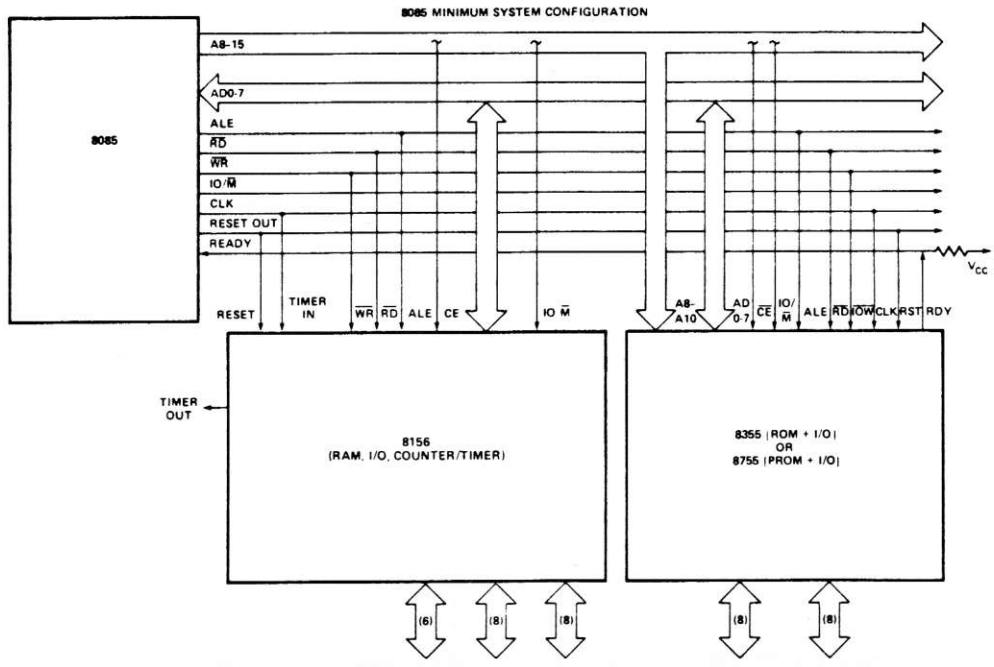


FIGURE 4. MCS-85™ MINIMUM SYSTEM (MEMORY MAPPED I/O)

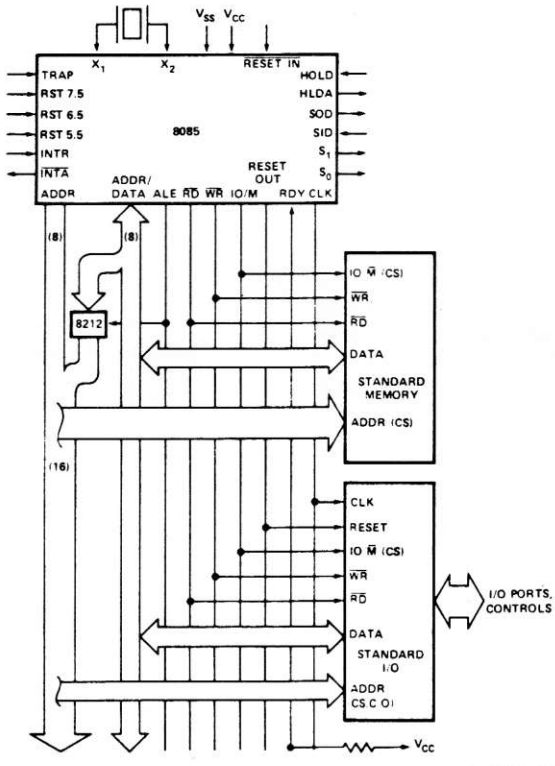
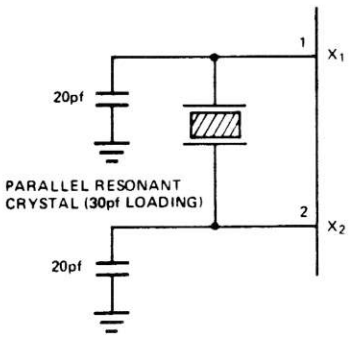


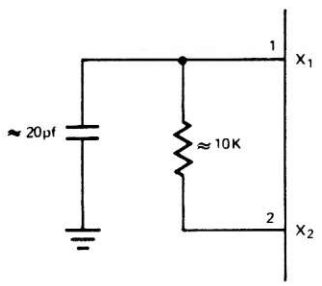
FIGURE 5. MCS-85™ SYSTEM (USING STANDARD MEMORIES)

DRIVING THE X_1 AND X_2 INPUTS

The user may drive the X_1 and X_2 inputs of the 8085 with a crystal, an external clock source or an RC network as shown below:

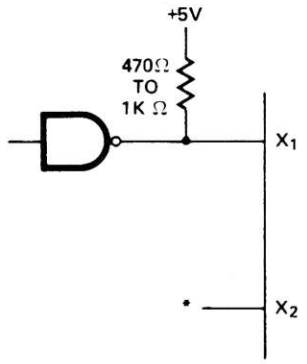


1-6 MHz
INPUT FREQUENCY



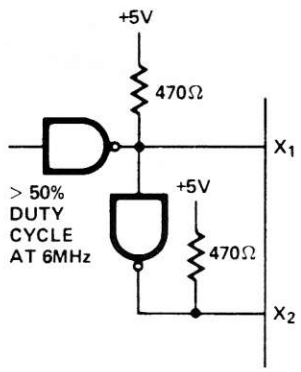
≈ 3 MHz
INPUT FREQUENCY

RC Mode causes a large drift in clock frequency because of the variation in on-chip timing generation parameters. Use of RC Mode should be limited to an application, which can tolerate a wide frequency variation.



1-6 MHz
INPUT FREQUENCY

(DUTY CYCLE AT 6MHz: 25 ~ 50%)
*WITH AN EXTERNAL CLOCK SOURCE
X_2 SHOULD BE LEFT FLOATING.



~6 MHz
INPUT FREQUENCY

This circuit may be used when the clock input has > 50% duty cycle at 6MHz.

FIGURE 6. DRIVING THE CLOCK INPUTS (X_1 AND X_2) OF 8085

GENERATING 8085 WAIT STATE

The following circuit may be used to insert one WAIT state in each 8085 machine cycle.

The D flip flops should be chosen such that
- CLK is rising edge triggered
- CLEAR is low-level active.

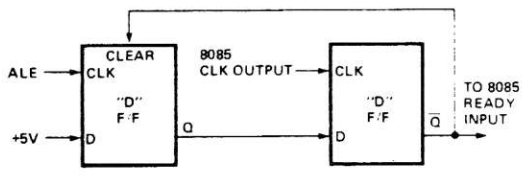


FIGURE 7. GENERATION OF A WAIT STATE FOR 8085 CPU

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.3 to +7V
Power Dissipation . . . . . 1.5 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

Bus Timing Specification as a T_{CYC} Dependent

t_{AL}	–	(1/2) T - 50	MIN
t_{LA}	–	(1/2) T - 60	MIN
t_{LL}	–	(1/2) T - 40	MIN
t_{LCK}	–	(1/2) T - 60	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 200	MAX
t_{RAE}	–	(1/2) T - 60	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T – 60	MIN
t_{WD}	–	(1/2) T - 80	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 30	MAX
t_{HABE}	–	(1/2) T + 30	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{INS}	–	(1/2) T + 200	MIN

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
T_{CYC}	CLK Cycle Period	320	2000	ns	See notes 1, 2, 3, 4, 5
t_1	CLK Low Time	80		ns	
t_2	CLK High Time	120		ns	
t_r, t_f	CLK Rise and Fall Time		30	ns	
t_{AL}	Address Valid Before Trailing Edge of ALE	110		ns	
t_{LA}	Address Hold Time After ALE	100		ns	
t_{LL}	ALE Width	120		ns	
t_{LCK}	ALE Low During CLK High	100		ns	
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns	
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0	ns	
t_{AD}	Valid Address to Valid Data In		575	ns	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		280	ns	
t_{RDH}	Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	0		ns	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	120		ns	T_{CYC} = 320ns; C_L = 150 pF
t_{CA}	Address (A8–A15) Valid After Control	120		ns	
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		ns	
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	80		ns	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400		ns	
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns	
t_{ARY}	READY Valid From Address Valid		220	ns	
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		ns	
t_{RYH}	READY Hold Time	0		ns	
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		ns	
t_{HABF}	Bus Float After HLDA		190	ns	
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns	
t_{AC}	Address Valid to Leading Edge of Control	270		ns	
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns	
t_{HDH}	HOLD Hold Time	0		ns	
t_{INS}	INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	360		ns	
t_{INH}	INTR Hold Time	0		ns	

NOTES:
1. A8-15 Address Specs apply to IO/$\overline{M}$, S0 and S1.
2. For all output timing where $C_L \neq 150pf$ use the following correction factors:
   $25pf \leq C_L < 150pf$: -.10 ns/pf
   $150pf < C_L \leq 300pf$: +.30 ns/pf
3. Output timings are measured with purely capacitive load.
4. All timings are measured at output voltage V_L = .8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
5. To calculate timing specifications at other values of T_{CYC} use the table in Table 2.
6. L.E. = Leading Edge T.E. = Trailing Edge

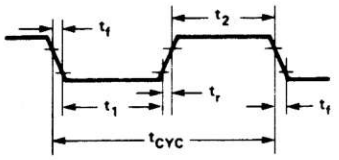
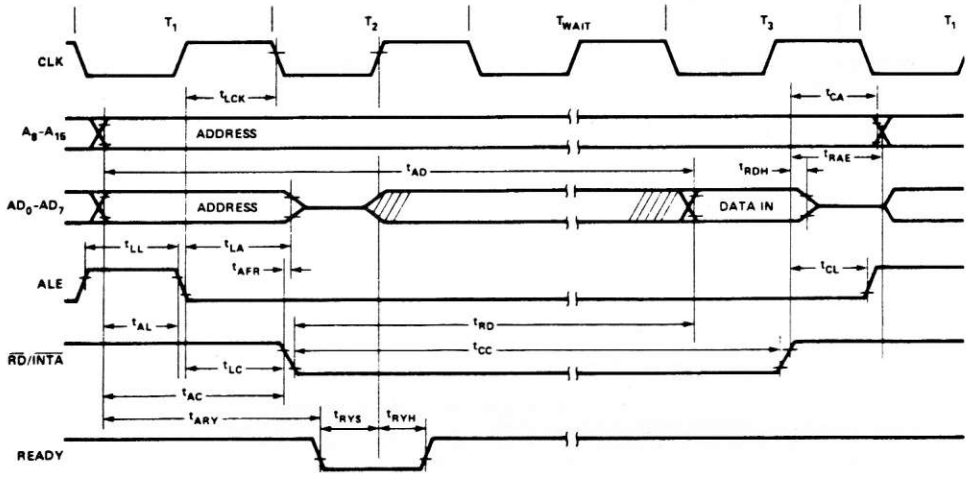


FIGURE 8. CLOCK TIMING WAVEFORM

READ OPERATION



WRITE OPERATION

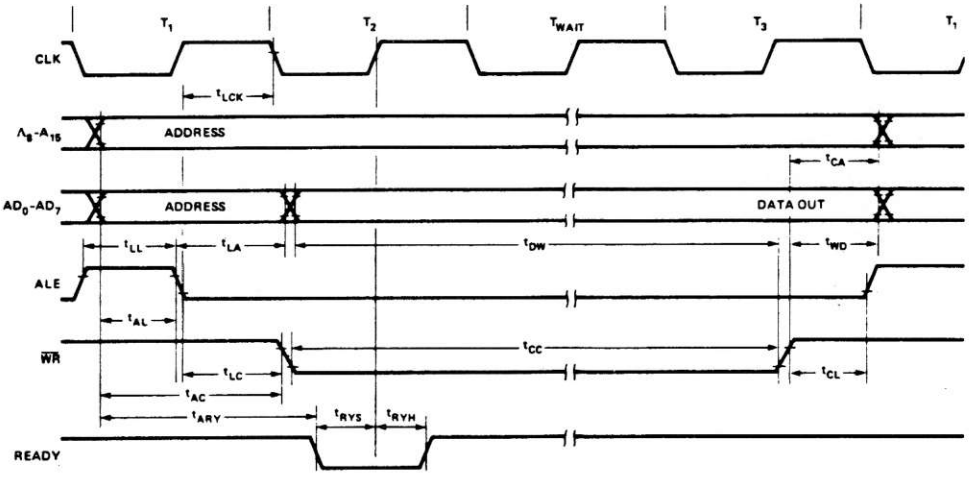


FIGURE 9. 8085 BUS TIMING

HOLD OPERATION

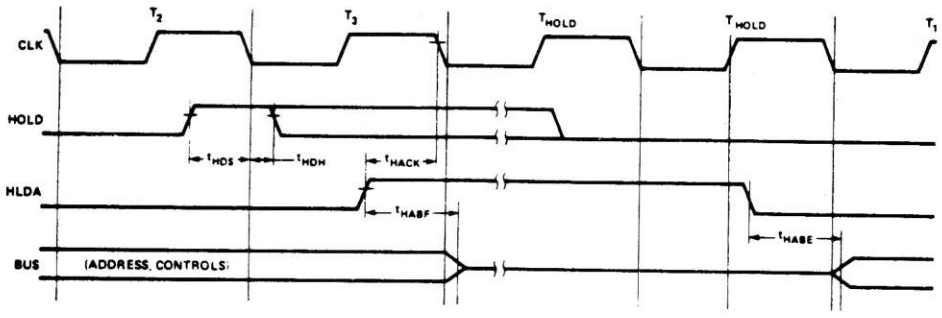


FIGURE 10. 8085 HOLD TIMING

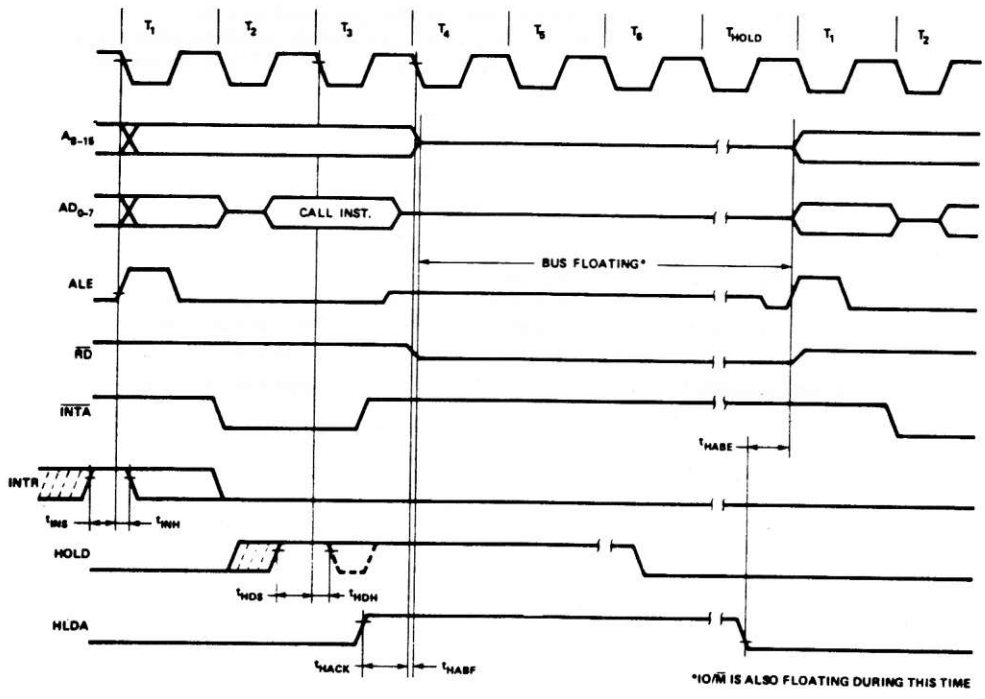


FIGURE 11. 8085 INTERRUPT AND HOLD TIMING

2716*
16K (2K x 8) UV ERASABLE PROM

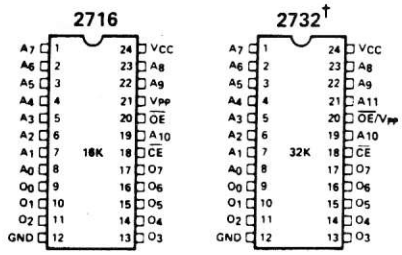
- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 5V ROMs (2316E, 2332, and 2364) and 2732 EPROM**
- **Simple Programming Requirements Single Location Programming Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's pin-for-pin compatible 16K ROM (the 2316E) or the new 32K and 64K ROMs (the 2332 and 2364 respectively).

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time – either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION*



†Refer to 2732 data sheet for specifications

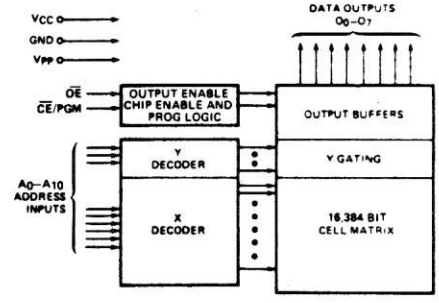
PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



Pin 18 and pin 20 have been renamed to conform with the entire family of 16K, 32K, and 64K EPROMs and ROMs. The die, fabrication process, and specifications remain the same and are totally uneffected by this change.

ɜRAMMING

ramming specifications are described in the Data Catalog PROM/ROM Programming Insutrctions on Page 4-83.

te Maximum Ratings*

rature Under Bias . . . . . -10°C to +80°C
ɹe Temperature . . . . . -65°C to +125°C
ıput or Output Voltages with
Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect
to Ground During Program . . . . . +26.5V to -0.3V

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply [1,2]	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Power Supply [2]	V_{CC} ± 0.6V [3]	V_{CC} ± 0.6V [3]	V_{CC} ± 0.6V [3]

PROM/ROM

READ OPERATION

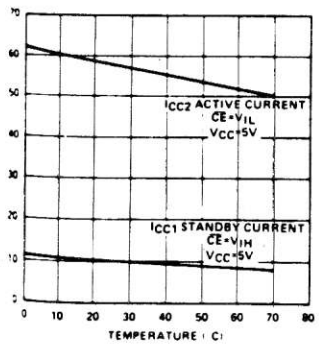
D.C. and Operating Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1} [2]	V_{PP} Current			5	mA	V_{PP} = 5.85V
I_{CC1} [2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2} [2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

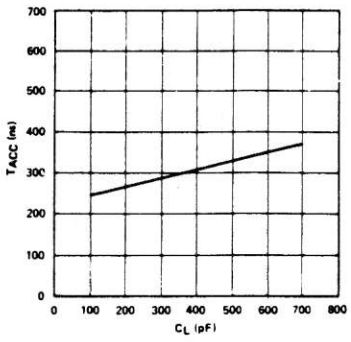
ɴOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.

Typical Characteristics

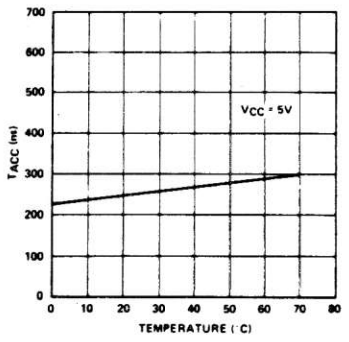
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

Symbol	Parameter	2716 Limits			2716-1 Limits			2716-2 Limits			Unit	Test Conditions
		Min	Typ[4]	Max	Min	Typ[4]	Max	Min	Typ[4]	Max		
t_{ACC}	Address to Output Delay			450			350			390	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			450			350			390	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120			120			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	0		100	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Address to Output Hold	0			0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

PROM/ROM

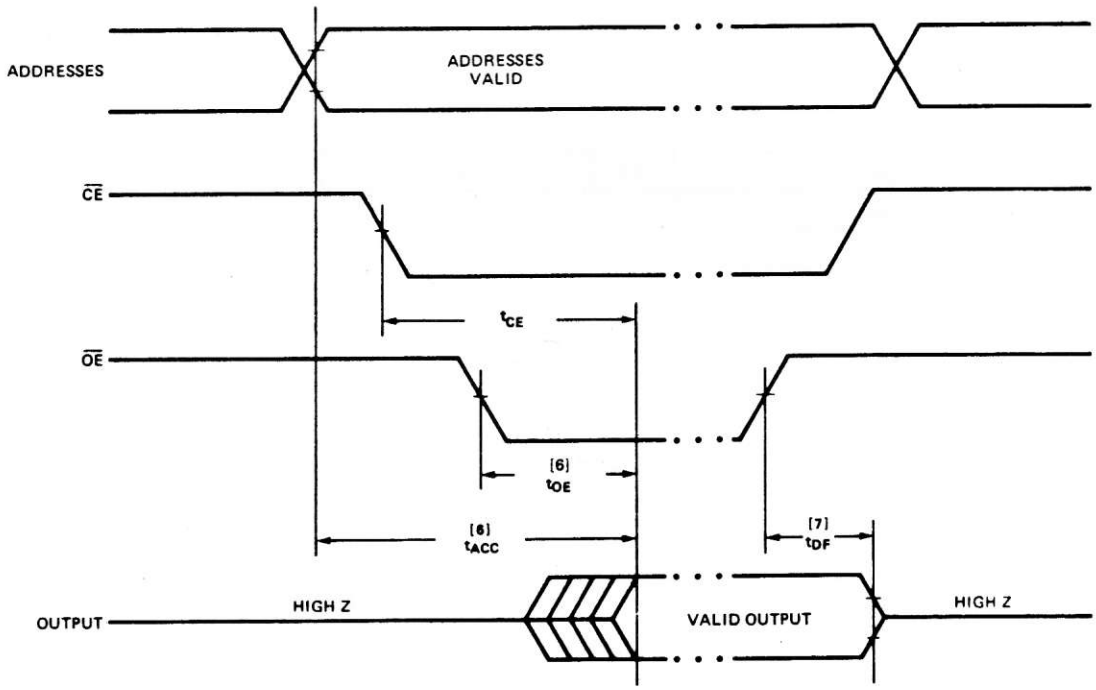
Capacitance[5] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

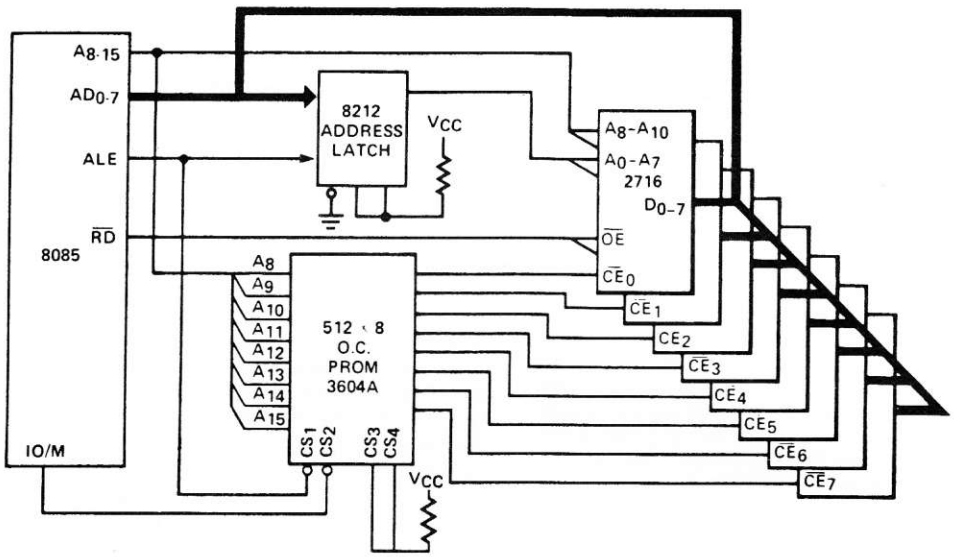
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms (1)



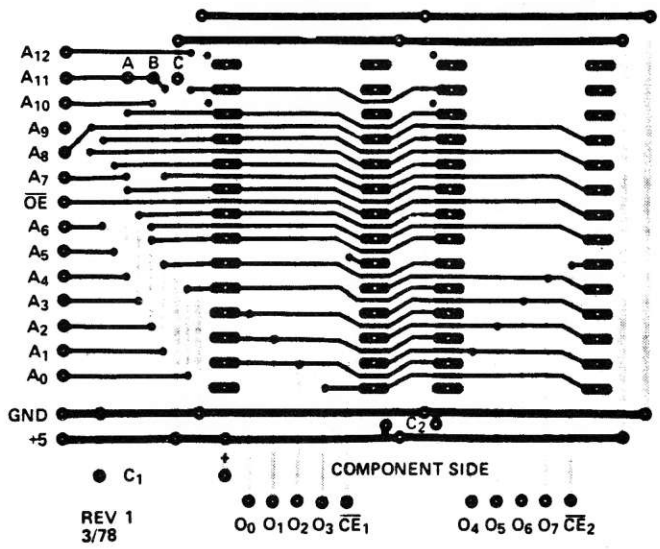
NOTE: 1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. Vpp may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the Vpp supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for $T_A = 25°C$ and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.
6. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

TYPICAL 16K EPROM SYSTEM



- This scheme accomplished by using $\overline{CE}$ (PD) as the primary decode. $\overline{OE}$ (CS) is now controlled by previously unused signal. RD now controls data on and off the bus by way of $\overline{OE}$.
- A selected 2716 is available for systems which require $\overline{CE}$ access of less than 450 ns for decode network operation.
- The use of a PROM as a decoder allows for:
  a) ALE is required for Edge Enabled devices (32K and 64K), and is optional for 2716.
  b) Compatibility with upward (and downward) memory expansion.
  c) Easy assignment of ROM memory modules, compatible with PL/M modular software concepts.

8K, 16K, 32K, 64K 5V EPROM/ROM FAMILY
PRINTED CIRCUIT BOARD LAYOUT



ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog page 4-83) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT DESELECTION

The outputs of two or more 2716s may be OR-tied together on the same data bus. Only one 2716 should have its output selected ($\overline{OE}$ low) to prevent data bus contention between 2716s in this configuration. The outputs of the other 2716s should be deselected by raising the $\overline{OE}$ input to a TTL high level.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2716. A low level $\overline{CE}$/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed wth V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

Chapter 2
FUNCTIONAL DESCRIPTION

The UPI-41 microcomputer is an intelligent peripheral controller designed to operate in MCS-85, MCS-80, and MCS-48 systems. The UPI's architecture, illustrated in Figure 2-1, is based on a low cost, single-chip microcomputer with program memory, data memory, CPU, I/O, event timer and clock oscillator in a single 40-pin package. Special interface registers are included which enable the UPI to function as a peripheral to an 8-bit master processor.

This chapter provides a basic description of the UPI microcomputer and its system interface registers. Unless otherwise noted the descriptions in this section apply to both the 8741 (with UV erasable program memory) and the 8041 (with factory mask programmed memory). These two devices are so similar that they can be considered identical under most circumstances. All functions described in this chapter apply to both the 8041 and 8741.

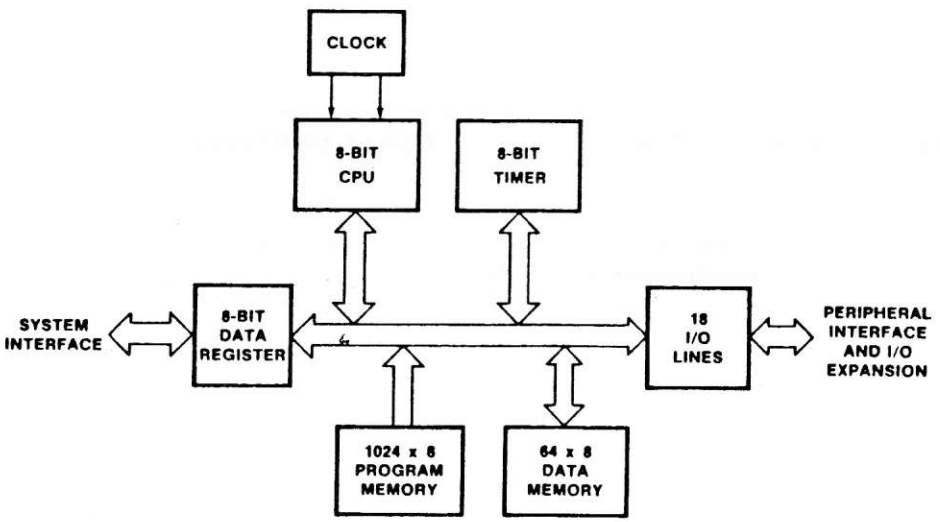


Figure 2-1. UPI-41 SINGLE CHIP MICROCOMPUTER

FUNCTIONAL DESCRIPTION

PIN DESCRIPTION

The 8741 and 8041 are packaged in 40-pin Dual In-Line (DIP) packages. The pin configuration for both devices is shown in Figure 2-2. Figure 2-3 illustrates the UPI Logic Symbol.

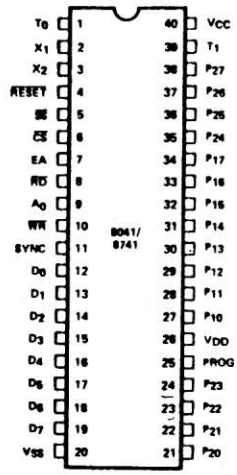


Figure 2-2. PIN CONFIGURATION

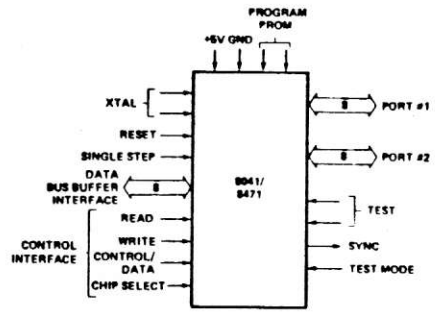


Figure 2-3. LOGIC SYMBOL

The following section summarizes the functions of each UPI-41 pin. NOTE that several pins have two or more functions which are described in separate paragraphs.

FUNCTIONAL DESCRIPTION

Pin Description (Refer to Figure 2-2)

Signal	Pin No.	Description
D_0–D_7	12–19	Three-state, bidirectional, DATA BUS BUFFER lines used to interface the UPI to an 8-bit master system data bus.
P_{10}–P_{17}	27–34	8-bit, PORT 1, quasi-bidirectional I/O lines.
P_{20}–P_{27}	21–24	8-bit, PORT 2, quasi-bidirectional I/O lines.
	35–38	The lower 4 bits (P_{20}–P_{23}) also interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access.
$\overline{WR}$	10	I/O write input which enables the master CPU to write data and commands to the UPI's DATA BUS BUFFER registers.
$\overline{RD}$	8	I/O read input which enables the master CPU to read data and status words from the DATA BUS BUFFER register and STATUS register.
$\overline{CS}$	6	Chip select input used to select one UPI out of several connected to common data bus.
A_0	9	Address input used by the master processor to indicate whether byte transfer is data (A_0=0) or command (A_0=1).
T0	1	Input pin which can be directly tested using conditional branch instructions. T0 is also used during PROM programming and verification in the 8741.
T1	39	Input pin which can be directly tested using conditional branch instructions. T1 also functions as the event timer input (under software control).
X1,X2	2,3	Inputs for a crystal, L-C or external timing signal to determine internal oscillator frequency.
SYNC	11	Output signal which occurs once per UPI instruction cycle. SYNC can be used as a strobe for external circuitry and it is also used to synchronize single step operation.
EA	7	External access input which allows emulation and testing of the UPI. EA is also used in PROM program verification.
PROG	25	Multifunction pin used as the program pulse input during PROM programming. During I/O expander operation the PROG pin acts as an address/data strobe to the 8243.
$\overline{RESET}$	4	Input used to reset status flip-flops and to set the program counter to zero. $\overline{RESET}$ is also used during PROM programming and verification.

FUNCTIONAL DESCRIPTION

Signal	Pin No.	Description
$\overline{SS}$	5	Single step input (8741 only) used in conjunction with the SYNC output to step the program through each instruction.
V_{CC}	40	+5V power supply pin.
V_{DD}	26	+5V during normal operation. Programming supply pin during PROM programming. Low Power standby pin in ROM version.
V_{SS}	20	Circuit ground potential.

FUNCTIONAL DESCRIPTION

ARCHITECTURE

The following sections provide a detailed functional description of the UPI microcomputer. Figure 2-4 illustrates the functional blocks within the UPI device.

CPU SECTION

The CPU section of the 8041 performs basic data manipulations and controls data flow throughout the single chip computer via the internal 8-bit data bus. The CPU section includes the following functional blocks shown in Figure 2-4:

- Arithmetic Logic Unit (ALU)
- Instruction Decoder
- Accumulator
- Flags

Arithmetic Logic Unit (ALU)

The ALU is capable of performing the following operations:

ADD with or without carry
AND, OR, and EXCLUSIVE OR
Increment, Decrement
Bit complement
Rotate left or right
Swap
BCD decimal adjust

In a typical operation data from the accumulator is combined in the ALU with data from some other source on the 8041 internal bus (such as a register or an I/O port). The result of an ALU

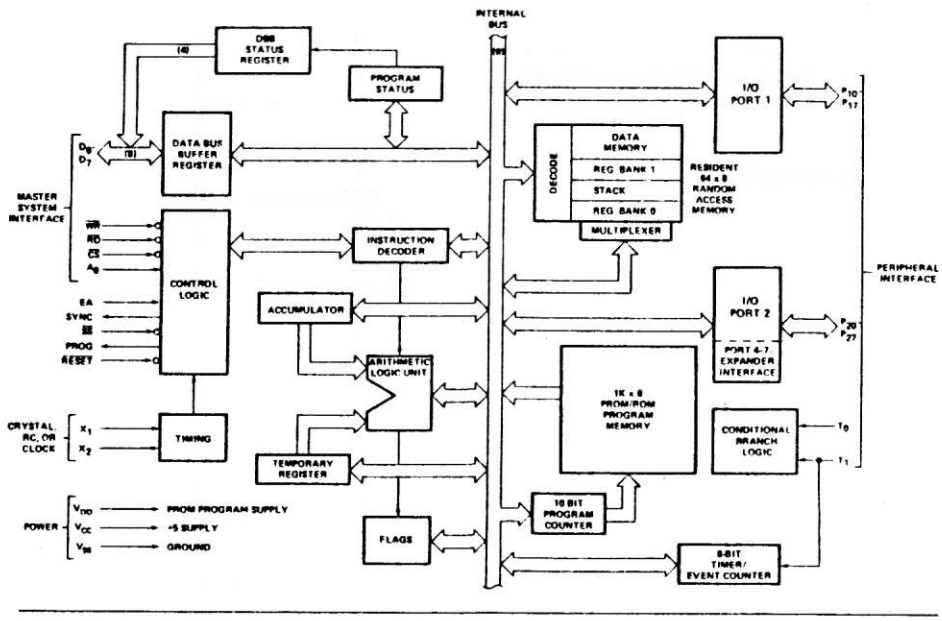


Figure 2-4. UPI BLOCK DIAGRAM

operation can be transferred to the internal bus or back to the accumulator.

If an operation such as an ADD or ROTATE requires more than 8 bits, the CARRY flag is used as an indicator. Likewise, during decimal adjust and other BCD operations the AUXILIARY CARRY flag can be set and acted upon. These flags are part of the Program Status Word (PSW).

Instruction Decoder

During an instruction fetch, the operation code (op-code) portion of each program instruction is stored and decoded by the instruction decoder. The decoder generates outputs used along with various timing signals to control the functions performed in the ALU. Also, the instruction decoder controls the source and destination of ALU data.

Accumulator

The accumulator is the single most important register in the processor. It is the primary source of data to the ALU and is often the destination for results as well. Data to and from the I/O ports and memory normally passes through the accumulator.

PROGRAM MEMORY

The UPI-41 has 1024 8-bit words of resident, read-only memory for program storage. Each of these memory locations is directly addressable by a 10-bit program counter. Depending on the type of application and the number of program changes anticipated, two types of program memory are available:

8041 with mask programmed ROM Memory
8741 with electrically programmable EPROM Memory

The 8041 and 8741 are functionally identical parts and are completely pin compatible. The 8041 has ROM memory which is mask programmed to user specification during fabrication.

The 8741 is electrically programmed by the user using the Universal PROM Programming (UPP) Module. It can be erased using ultraviolet light and reprogrammed at any time.

A program memory map is illustrated in Figure 2-5. Memory is divided into 256 location 'pages' and three locations are reserved for special use:

Location 0

Following a RESET input to the processor, the next instruction is automaticaly fetched from location 0.

Location 3

An interrupt generated by an Input Buffer Full (IBF) condition (when the IBF interrupt is enabled) causes the next instruction to be fetched from location 3.

Location 7

A timer overflow interrupt (when enabled) will cause the next instruction to be fetched from location 7.

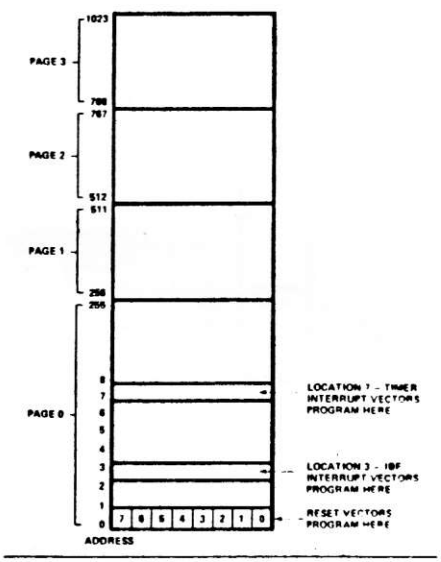


Figure 2-5. PROGRAM MEMORY MAP

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION

HM-6514

1024 x 4 CMOS RAM

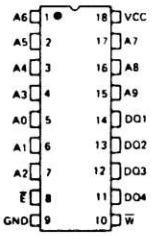
DECEMBER 1977

Features

- LOW POWER STANDBY . . . . . ≪ 1mW MAX.
- LOW POWER OPERATION . . . . . 35mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



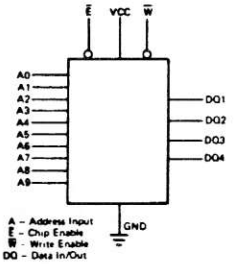
Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

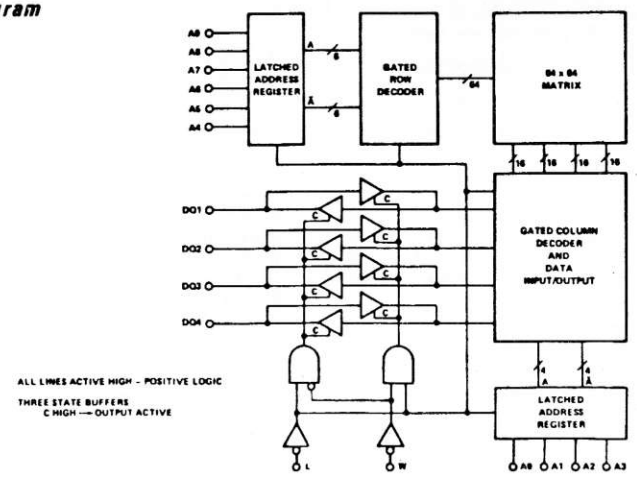
On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



Specifications HM-6514-2/HM-6514-9

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage – VCC	+8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Industrial (-9)	4.75 V to 5.25V
		Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V MIN	TEMP = 25°C ① VCC = 5.0V TYP	TEMP = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	µA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VI = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		170	250	NS	④
	TAVQV	Address Access Time		320		170	270	NS	④
	TELQX	Chip Enable Output Enable Time		100		50	80	NS	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	NS	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	NS	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		NS	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		NS	④
	TAVEL	Address Setup Time	20		20	0		NS	④
	TELAX	Address Hold Time	50		50	20		NS	④
	TWLWH	Write Enable Pulse Width	300		240	150		NS	④
	TWLEH	Write Enable Pulse Setup Time	300		240	150		NS	④
	TELWH	Write Enable Pulse Hold Time	300		240	150		NS	④
	TDVWH	Data Setup Time	200		160	100		NS	④
	TWHDZ	Data Hold Time	0		0	0		NS	④
	TWHEL	Write Enable Read Setup Time	0		0	0		NS	④
	TQVWL	Data Valid to Write Time	0		0	0		NS	④
	TWLDV	Write Data Delay Time	100		80	50		NS	④
	TELWL	Early Output High-Z Time		0		0	0	NS	④
	TWHEH	Late Output High-Z Time		0		0	0	NS	④
	TELEL	Read or Write Cycle Time	420		350	240		NS	④

NOTES
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20ns; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

Specifications HM-6514-5

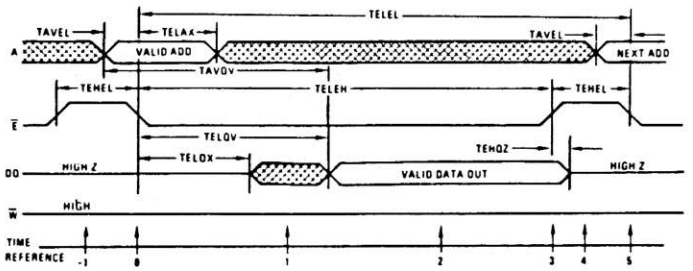
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage – VCC	+8.0V	Operating Supply Voltage Commercial	4.75V to 5.25V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Operating Temperature Commercial	0°C to +75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.1	1.0	mA	VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		8.0	10.0	pF	VI = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	NS	④
	TAVQV	Address Access Time		370		200	320	NS	④
	TELQX	Chip Enable Output Enable Time		100		50	80	NS	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	NS	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	NS	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		NS	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		NS	④
	TAVEL	Address Setup Time	20		20	0		NS	④
	TELAX	Address-Hold Time	50		50	20		NS	④
	TWLWH	Write Enable Pulse Width	350		300	200		NS	④
	TWLEH	Write Enable Pulse Setup Time	350		300	200		NS	④
	TELWH	Write Enable Pulse Hold Time	350		300	200		NS	④
	TDVWH	Data Setup Time	250		220	150		NS	④
	TWHDZ	Data Hold Time	0		0	0		NS	④
	TWHEL	Write Enable Read Setup Time	0		0	0		NS	④
	TDVWL	Output Data Valid to Write Time	0		0	0		NS	④
	TWLDV	Write Data Delay Time	100		80	50		NS	④
	TELWL	Early Output High-Z Time		0		0	0	NS	④
	TWHEH	Late Output High-Z Time		0		0	0	NS	④
	TELEL	Read or Write Cycle Time	500		420	320		NS	④

NOTES: 1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

Read Cycle

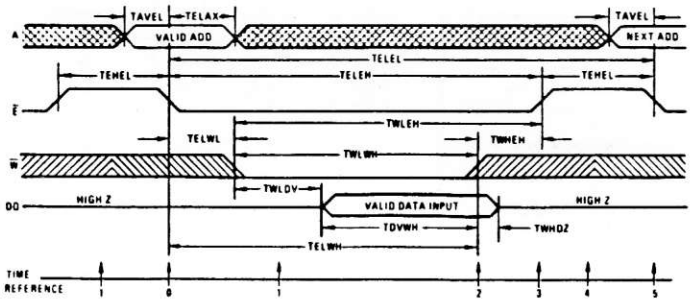


TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	DATA I/O DQ	FUNCTION
1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



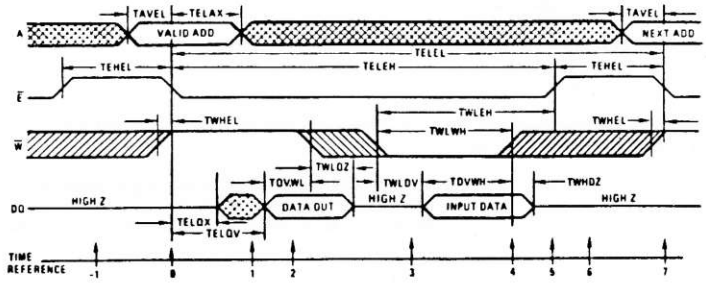
TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in on chip registers. If a dedicated write cycle is to be performed and the outputs are not to become active TELWL and TWHEH must be met. Under these conditions TWLDV is unnecessary and input data may be applied at any convenient time as long as TDVWH is still met. If TELWL is not met then the outputs may become enabled momentarily near the beginning of the cycle and a disable time (TELQZ + TWLDV) must be met before the input data is applied (TWLQZ + TWLDV). Similarly, if TWHEH is not met the outputs may enable briefly near the end of the cycle.

The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum required $\overline{E}$ high time (TEHEL) the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

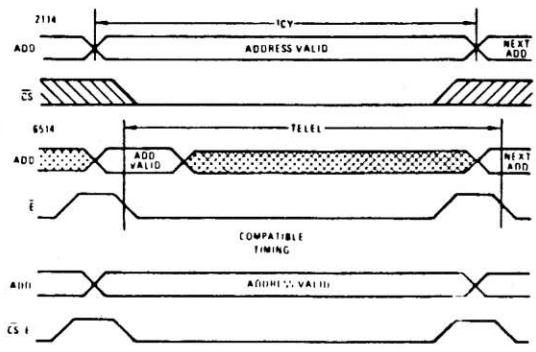
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DO	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS. ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE. OUTPUT ENABLED
2	L	H	X	V	READ MODE. OUTPUT VALID
3	L	L	X	Z	WRITE MODE. OUTPUT HIGH Z
4	L	↘	X	V	WRITE MODE. DATA IS WRITTEN
5	↘	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS. NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2114 Compatibility



2114 – Requires the Address to Remain Valid Throughout the Cycle.

6514 – Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

Battery Backup Applications

The HM-6514 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6595, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75 volts).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF $\approx$.2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the R/W circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

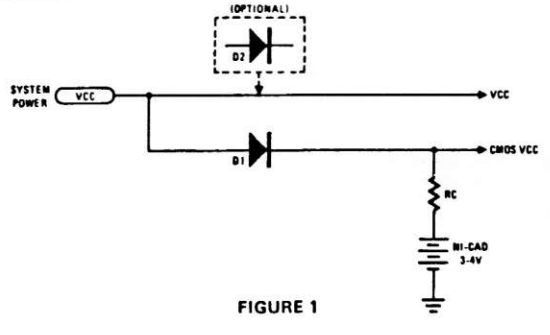


FIGURE 1

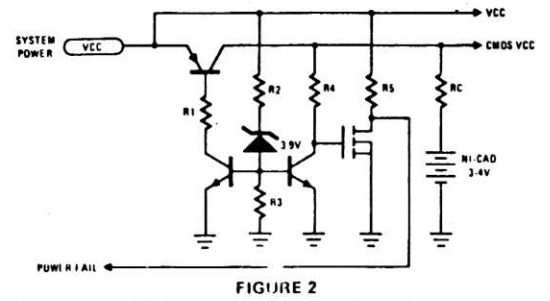


FIGURE 2

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

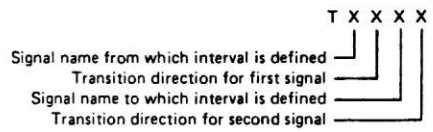
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL – Input Low Voltage
IOZ – Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



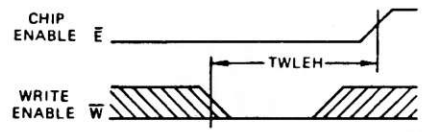
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

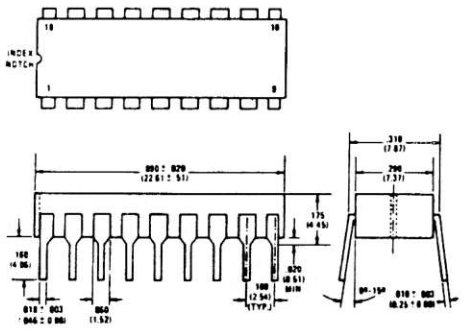
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

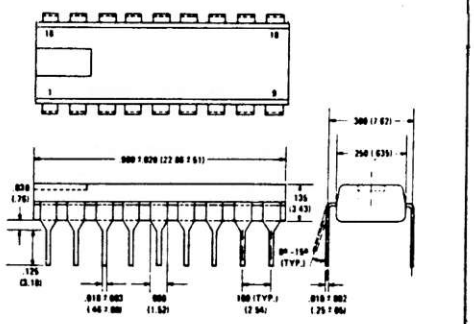
WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

Packaging

18 LEAD CERAMIC D.I.P.



18 LEAD EPOXY D.I.P.



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Ordering Information

Example: HM 1 – 6514 – 9

- HARRIS MEMORY
- PACKAGE
- DEVICE
- VERSION/TEMP. RANGE

TEMPERATURE RANGE

PACKAGE		MILITARY -2	INDUSTRIAL -9	COMMERCIAL -5
FLAT PACK	9-	YES	NO	NO
CERDIP	1-	YES	YES	YES
EPOXY	3-	NO	YES	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION

SWITCHED MODE POWER SUPPLY CONTROL UNIT — TDA1060

TDA1060-N

DESCRIPTION

The TDA1060 is a monolithic integrated circuit intended for the control of switched mode power supplies. It incorporates all the control and protection functions likely to be required in switched mode power supplies for professional equipment.

FEATURES

- **Stabilized power supply**
- **Temperature compensated voltage reference**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote ON/OFF switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/over voltage protection**
- **Maximum duty cycle adjustment**
- **External synchronization input**
- **Feed forward**

FUNCTIONAL DESCRIPTION

A. Stabilized Power Supply

The circuit can be fed either by a current source (e.g. connected to the high voltage input of the SMPS via a series resistor), or a voltage source (e.g. a 12V battery). When fed from a 12V supply the maximum current consumption is 10mA.

The stabilized voltage is typically 8.4V and is available on pin 2 for supplying external circuitry. Up to 5mA can be drawn from this supply whereupon the total IC current consumption increases by the same amount. This stabilized supply is protected against short circuits.

B. Reference Voltage Source

The reference voltage for the SMPS is incorporated in the IC. The temperature stability of this reference is ±100ppm/°C maximum.

C. Sawtooth Generator and Feed Forward

The frequency of the sawtooth generator is set by an external resistor (pin 7) and a capacitor (pin 8). The frequency can be determined with the aid of Figure 3. It may be set between 50Hz and 100KHz and is virtually independant of supply voltage.

The upper and lower levels of the sawtooth are fixed by an internal resistor divider. Since these resistors form a bridge configuration with the external voltage divider for the δ-max setting; the accuracy of the δ-max setting is determined by resistor matching rather than by absolute values.

During the flyback of the sawtooth the output pulse is inhibited. This acts as an internal duty cycle limiter. Since the flyback time is 1μs (with 1nF capacity), the maximum duty cycle is limited to 95% at 50KHz.

The frequency of the sawtooth can be synchronized via the TTL-compatible input on pin 9. The synchronizing frequency must be lower than the oscillator free running frequency. When the input on pin 9 is Low the sawtooth generator is stopped, starting again when the input goes High. For free-running operation pin 9 is left dissconnected.

Feed forward can be provided via pin 16 which has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on pin 16 increased the upper level of the sawtooth is also increased. Since neither the δ-max voltage level nor the feedback voltage are influenced by the feed forward; the duty cycle reduces. This is a linear function and can therefore compensate for supply voltage variations. If feed forward is not required pin 16 should be connected to pin 12.

D. Feedback Amplifier

The difference between the feedback voltage (pin 3) and the internal reference voltage is amplified in an operational amplifier. The output signal is compared with the sawtooth which has an amplitude of typically 4.5V (without feed forward).

The gain can be controlled by a feedback circuit from the op. amp. output (pin 4). To avoid instability a capacitor should be connected across the op amp (i.e. between pins 3 and 4).

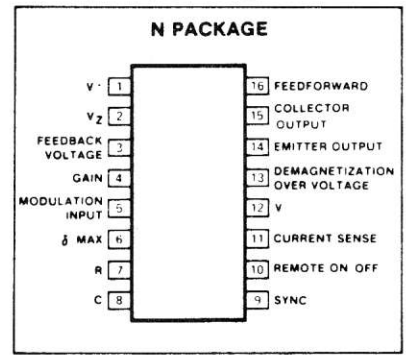
E. Remote ON/OFF

Remote switching can be provided through the TTL-compatible input on pin 10. When this input is Low the circuit is switched off. With the input High the circuit switches on via the slow start procedure.

F. Current Limiter

The current limiter comprises two comparators with trip-on levels of 480mV and 600mV respectively. When the voltage on the current sense input (pin 11) exceeds 480mV, the output pulse is immediately cut off, starting again at the next period. If the voltage exceeds 600mV, the output pulse is inhibited during a certain "dead time", during which the slow start capacitor is unloaded. After this the circuit starts again with slow start.

PIN CONFIGURATION



G. Low Supply Voltage Protection

When the supply voltage is too low (less than Vz + 0.2V) the circuit is automatically switched off. Starting takes place again via the slow start as soon as the supply voltage exceeds this threshold value.

H. Feedback Loop Fault Protection

If the feedback loop is open, the feedback input (pin 3) is pulled high by an internal current source making the duty cycle zero. If the feedback loop is short-circuited, or if the feedback voltage does not exceed 600mV, the δ-max pin is connected to the lower level of the sawtooth by a 1kΩ resistor. This causes a lower δ-max voltage as described in the maximum duty cycle and slow start section.

I. Output

The output circuit comprises a latch and an output transistor. Both collector and emitter of the output transistor are available on pins 15 and 14 respectively. The collector is internally connected to the supply voltage of the integrated circuit by a clamping diode to limit the output voltage in the case of a fault in the external drive circuit of the switching transistor.

J. Demagnetisation/Overvoltage

The demagnetisation/overvoltage input (pin 13) inhibits the output when the voltage at this pin exceeds the trip-on level of 600mV. The combined function can be realized by a zener diode from the output voltage of the SMPS to this pin (e.g. a 5.6 zener in a 5V supply) and the demagnetisation sensor connected also directly to this point.

K. Maximum Duty Cycle and Slow Start

The voltage on pin 6 (δ-max setting) determines the maximum output duty ratio. As explained in section C the δ-max setting accuracy is very good since the voltage at this pin is divided by a resistive divider from the Vz voltage.

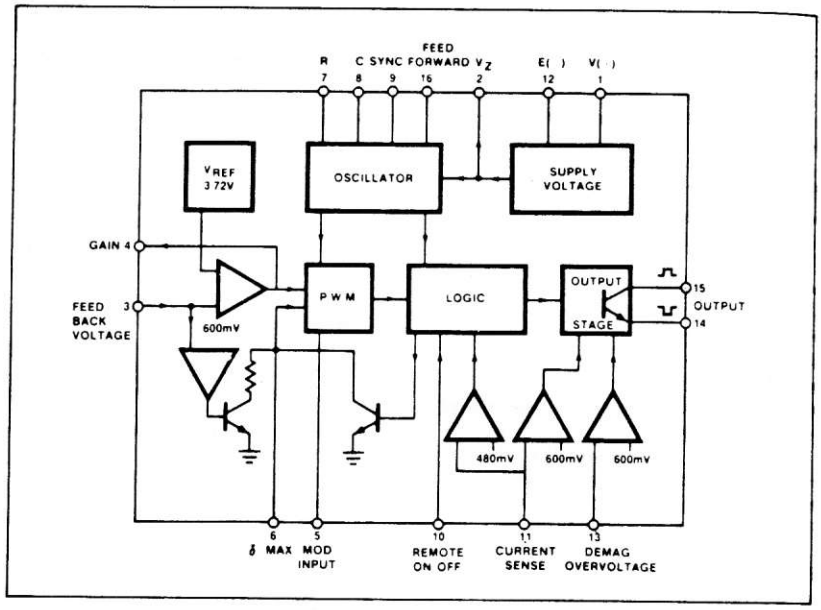
In the event of a loop fault the δ-max pin is connected via an internal 1kΩ resistor to the lower limit of the sawtooth voltage. Thus the δ-max value is decreased to a level determined by the impedance of the δ-max resistive divider to the internal 1kΩ.

The capacitor connected to the δ-max pin, together with the impedance of the resistive divider, determines the time constant for the slow start. For remote ON/OFF or when the current sensing voltage exceeds 600mV, the value of the capacitor determines the dead time of the slow start procedure.

L. Modulation Input

Pin 5 gives an input to the pulse width modulator which may be used for current mode regulation. The duty cycle reduces when the voltage at this point decreases.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING Min	RATING Max	UNIT
Vcc	Supply voltage	-0.5	18	V
Icc	Supply current	0	30	mA
	Output current	0	40	mA
	Voltages at the pins with respect to pin 12			
	Feed forward (pin 16)	0	V+	V
	Output emitter (pin 14)	0	5	V
	Output collector (pin 15)	0	V+	V
	All other inputs	0	V_Z	V
	Storage temperature	-25	+125	°C
	Operating temperature	-25	+85	°C

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DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = 12V (VP) unless otherwise specified.[1,2,3,4,5]

PARAMETER			TEST CONDITIONS	TDA1060			UNIT
				Min	Typ	Max	
V_{IN}		Input voltages					
	Pin 1		Current FED I_1 =10mA	20	21	23	V
	Pin 1		Current FED I_1 = 30mA	20	25	30	V
V_Z	Pin 2			7.8	8.4	9.0	V
ΔV_Z/temp.		V_Z drift		-1.3		1.3	mV/°C
	Pin 10	Remote ON/OFF[2]	Circuit ON	2		V_Z	V
	Pin 10	Remote ON/OFF[2]	Circuit OFF	0		0.8	V
	Pin 11	Inhibit	Single pulse inhibit.	0.76	0.8	0.84	V_{11}(Start)
	Pin 11	Start	Shutdown/slow start.	470	600	720	mV
	Pin 3	Feedback loop protection	Trip on	470	600	700	mV
	Pin 14	Maximum emitter voltage		5			V
	Pin 14-15	Saturation voltage	I_{15} = 40mA			400	mV
	Pin 13	Over voltage input[4]	Trip on level	470	600	720	mV
	Pin 6	δ-max voltage level	Duty cycle = 50% (15-50kHz)	0.38V_Z	0.4V_Z	0.42V_Z	V
	Pin 9	Synchronization input	Sawtooth stopped	0		0.8	V
	Pin 9	Synchronization input	Sawtooth running	2		V_Z	V
V_{REF}	Reference voltage			3.42	3.72	4.03	V
ΔV_{REF}	Temperature coefficient of reference voltage			-100		100	ppm/°C
	Lower sawtooth level				1.1		V
	Upper sawtooth level				5.6		V
V_{PT}	Supply voltage protection		Trip-on level	V_Z+.2		V_Z+1.7	V
ΔV_{PT}	Supply voltage protection Temperature coefficient			-6.5			mV/°C
I_{IN}	Input currents						
	Pin 1	Supply current	Voltage FED	5		10	mA
	Pin 2	Maximum allowable external current drain				5	mA
	Pin 3	Input current			-40		µA
	Pin 10	Sink current[2]	V_{10} = 0			-90	µA
	Pin 11	Input current	V_{11} = 250mV			12	µA
	Pin 15	Available output current		40			mA
I_{IN}		Input currents					
	Pin 13	Input current[4]	V_{13} = 250mV			10	µA
	Pin 6	Input current	V_6 = 1V			20	µA
	Pin 16	Input current				5	µA
	Pin 9	Sink current	V_9 = 0			-90	µA
	Pin 5	Input current	V_5 = 1V			-40	µA
R	Sawtooth resistor value			10		40	kΩ
R	Amplifier resistor value			100			kΩ
A_{VOL}	Amplifier open loop gain				60		dB
	Internal duty cycle limiting		Period time T µs c = 1nF			(T-1)/T	
	δ-max setting			0		(T-1)/T	

NOTES

1 The remote ON/OFF is not active when this pin is not connected.
2 The synchronization is not active when this pin is not connected.
3 The demagnetisation/overvoltage protection is active when this pin is not connected.
4 The current limiter is active when this pin is not connected.
5 All voltages with respect to pin 9.

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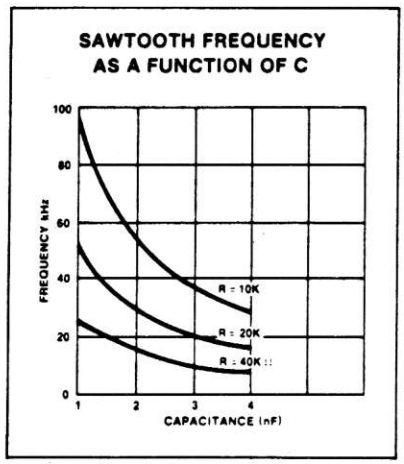
AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	TEST CONDITIONS	TDA1060			UNIT
					Min	Typ	Max	
T_D	Delay time	Output	Pin 11	25% overdrive, 40mA output current			0.8	µs
F	Sawtooth frequency range			Figure 3	0.05		100	kHz
$\Delta F/\Delta V$	Frequency drift with supply			8≤ V16 ≤ V+			2.3	%

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATION